Side Channel Analysis of AVR XMEGA

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CHES 2009 Rump Session

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  - inter-peripheral event system
  - ADC/DAC, EBI, SPI, TWI, PDI, WDT, IRCOM, AWeX, ...
  - advanced clocking options (PLL, DFLL)
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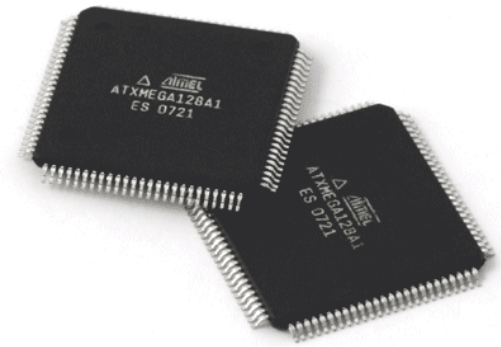
- reported use by [Rhode et al. CARDIS'08], [Eisenbarth et al. CHES'09]

XMEGA Crypto Engines

DES Instruction

- performs single DES round
- full DES in 17 clock cycles



AES Peripheral

- AES-128 in **375** clock cycles (vs. 3-4K cycles in software)
- around **10 Mbps** bandwidth at maximum clock speed
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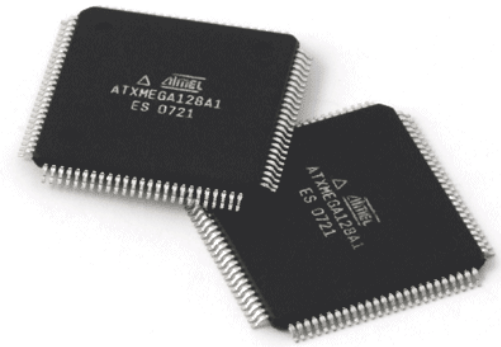

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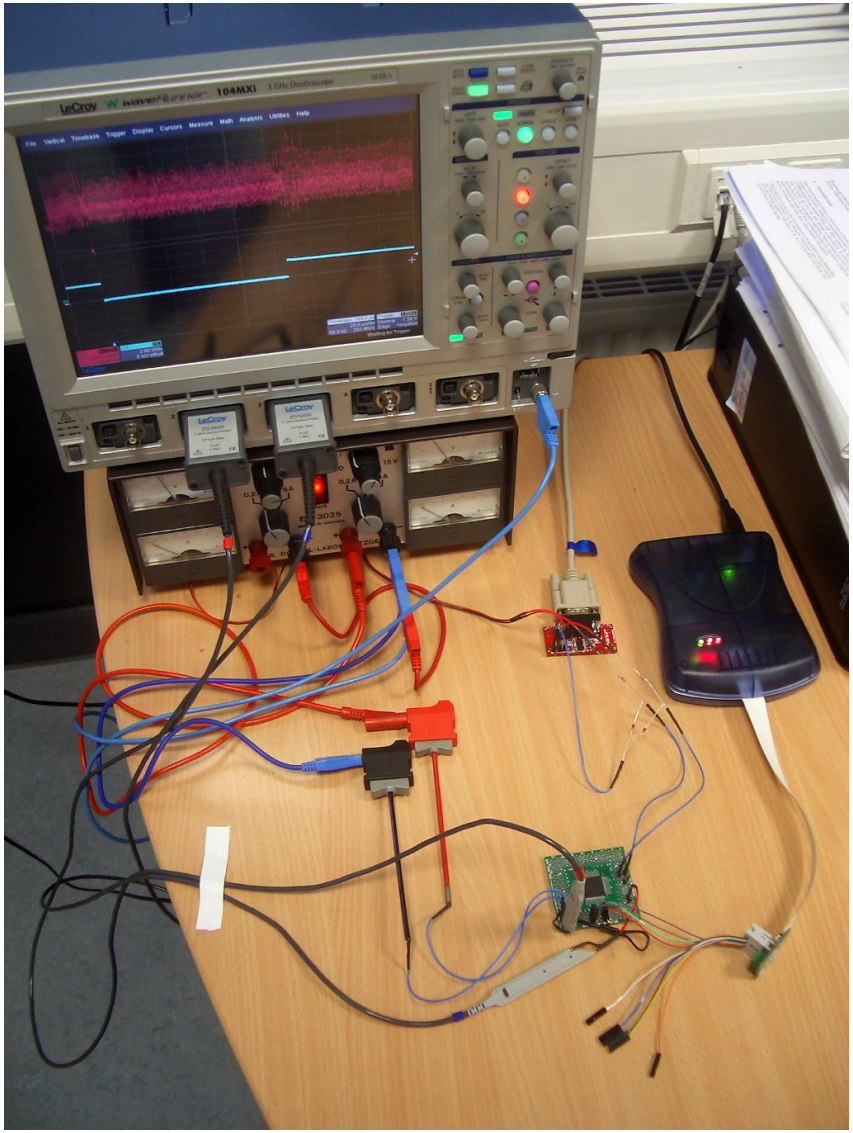
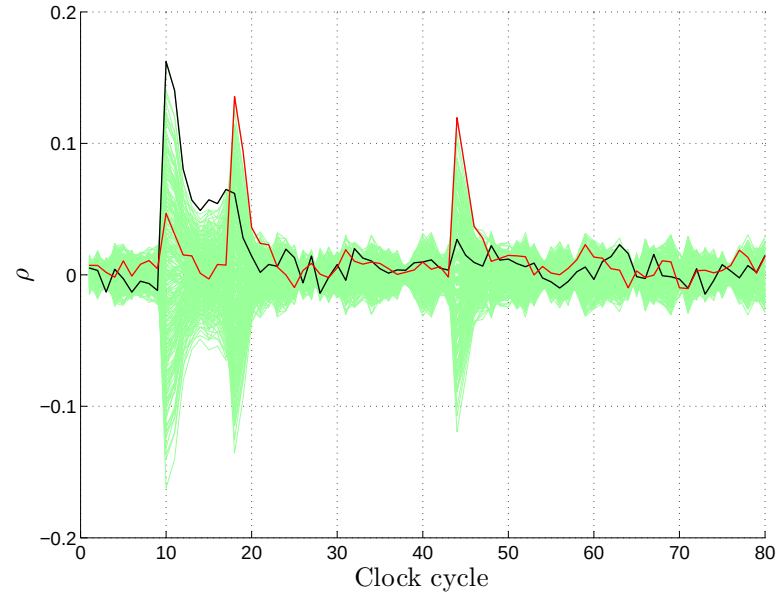
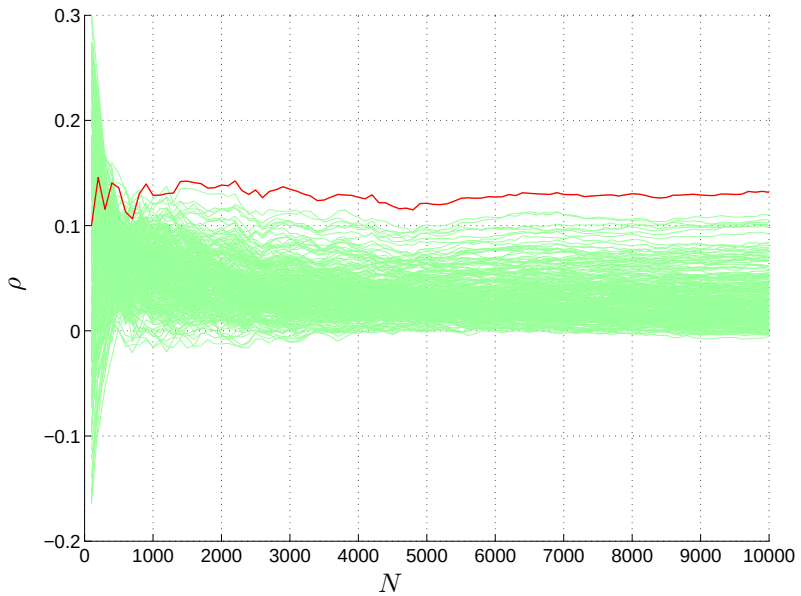
What about resistance to implementation attacks?

- no single word about countermeasures in the datasheet or anywhere else

Side-Channel Attack on XMEGA AES Engine



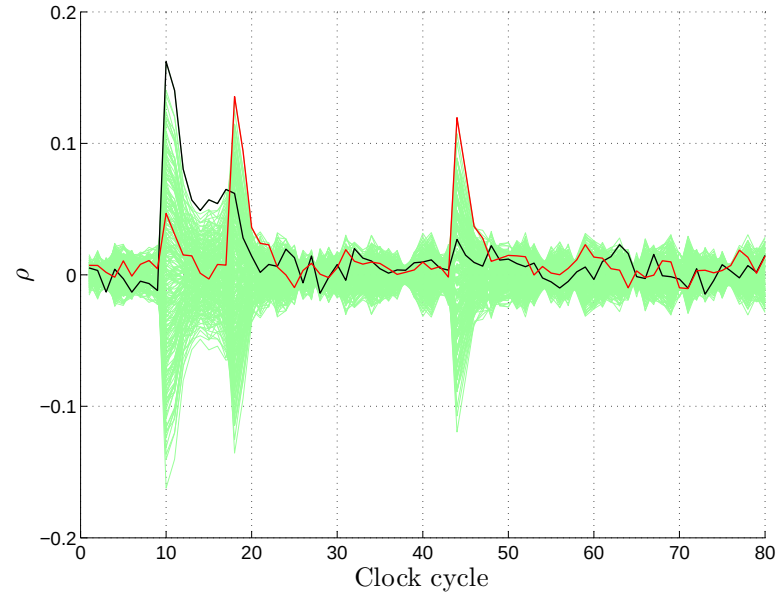


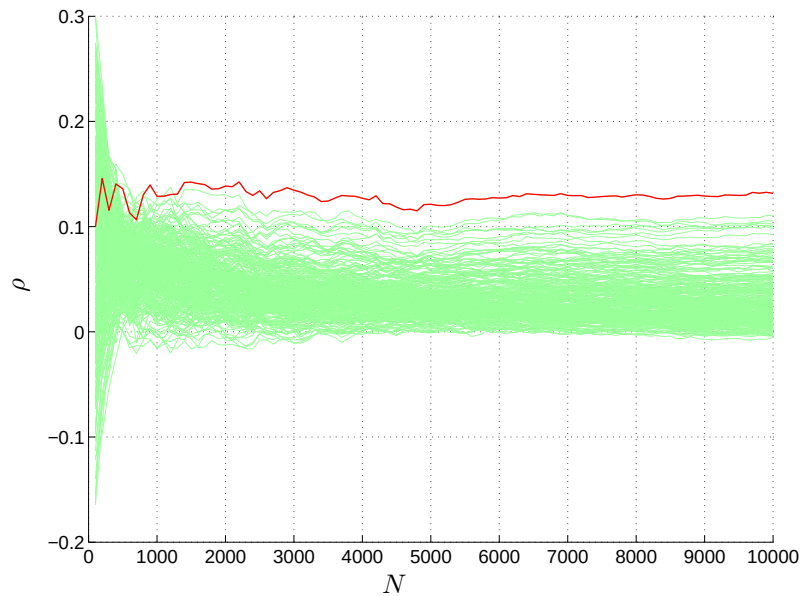


Side-Channel Attack on XMEGA AES Engine

Attack details

- CPA in HD leakage model
- **3000 power traces** for full 128-bit key recovery
- 100 MS/s sampling rate
- setup cost $\approx$ \$1000
- reveals that implementation is not parallel





Take care when using XMEGA crypto features

http://cryptolux.org/Implementation_attacks